ABSTRACT OF THE DISCLOSURE

A pixel has first to third N-type TFT elements serially connected between a data line and a pixel electrode node. Each gate of the first and second TFT elements is connected to a first gate line, while the gate of the third TFT element is connected to a second gate line. The first and second gate lines in a select state each set to a high voltage that can fully turn-on the first to third TFT elements. The first gate line in a non-select state is set to a low voltage that can fully turn-off the first and second TFT elements, while the second gate line in the non-select state is set to an intermediate voltage between the maximum and the minimum voltages being transmitted on the data line.